Code :9F00203

M.C.A-II Semester Supplementary Examinations, January 2011
COMPUTER ORGANIZATION
(For students admitted in 2009-2010 only)

Time: 3 hours **Max Marks: 60**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Convert the following decimal numbers to the bases indicated below.
   i. 7562 to octal
   ii. 1938 to hexadecimal
   iii. 175 to binary.
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2^1s complement of the subtrahend.
   i. 11010-10000
   ii. 1010100-1000011

2. (a) Simplify the following Boolean function using four-variable k-map.
   $F(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 10) + d\sum(5, 6, 11, 15)$
   (b) Design a 2-bit count-down counter. This is a sequential circuit with two flip-flops and one input n. When x=0, the state of the flip-flops does not change. When x=1, the state sequence is 11,10,00,11 and repeat.

3. (a) Explain about hardware organization, read and write operations of associative memory.
   (b) Briefly explain about cache memory.

4. (a) Write computer instruction format, microinstruction code format and explain each field of format with an example.
   (b) Briefly explain the design of control unit.

5. (a) What is the difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?
   (b) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part. Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

6. Write a short notes on:
   (a) Programmed I/O
   (b) Interrupt - initiated I/O
   (c) Direct memory access.

7. (a) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks and explain the operation.
   (b) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

8. Explain about inter processor arbitration techniques.

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